CLAIMS

What is claimed is:

1. A semiconductor device comprising:
- an active region of a first conducting type including a transistor structure,
- a ring shaped region of the first conducting type extending from a surface of the active region into the active region and substantially surrounding the transistor structure.

2. The device as in claim 1, wherein the transistor structure comprises, a drain region, a source region, wherein the drain and the source define a channel, a gate being arranged above said channel, and a sinker structure of said first conducting type arranged substantially along said source region reaching from the surface of the active area next to the source region to the bottom of the active area.

3. The device as in claim 2, wherein the p ring is less doped than the sinker structure.

4. The device as in claim 2, wherein the drain region comprises a lightly doped drain region.

5. The device as in claim 4, further comprising a metal layer on the backside of the semiconductor device.

6. The device as in claim 1, wherein the transistor structure is a two transistor structure comprising, a common drain region, a first source region arranged on one side of the common drain region, a second source region arranged on the respective opposite side of the drain region, wherein the drain region and the source regions each define a channel, a first and second gate being arranged above said channels, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area.

7. The device as in claim 5, wherein the drain region comprises a lightly doped drain region.

8. The device as in claim 5, further comprising a metal layer on the backside of the semiconductor device.

9. The device as in claim 5, wherein the ring is less doped than the sinker structure.

10. The device as in claim 1, wherein the ring is doped in the range of 10^{14}-$10^{15}/cm^2$.

11. The device as in claim 1, wherein the active area is created and enclosed by a LOCOS process.

12. The device as in claim 11, wherein the active area comprises a substrate and an epitaxial layer on top of said substrate.

13. The device as in claim 1, wherein the first conducting type is the p type.

14. The device as in claim 1, wherein the ring is created by masked ion implant.

15. The device as in claim 10 wherein boron is used as a dopant.

16. The device as in claim 1, wherein the ring has a rectangular, circular, oval, or polygon shape.

17. The device as in claim 1, wherein the ring comprises at least one gap that does not substantially influence an insulating function of the ring.

18. A semiconductor device comprising:
- an active region of a first conducting type including a transistor structure, wherein the transistor structure comprises, a drain region of a second type, a channel, and a gate being arranged above said channel, and
- a ring shaped region of the first conducting type extending from a surface of the active region into the active region and surrounding the transistor structure.

19. The device as in claim 18, further comprising a source region of the second type arranged along one side of the drain region, and a sinker structure of said first conducting type arranged substantially along said source region reaching from the surface of the active area next to the source region to the bottom of the active area.

20 The device as in claim 19, further comprising a second source region arranged on the respective opposite side of the drain region, wherein the drain region and the source regions each define a channel, a first and second gate being arranged above said channels, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area.

21. The device as in claim 18, wherein the drain region comprises a lightly doped drain region.

22. The device as in claim 19, further comprising a metal layer on the backside of the semiconductor device.

23. The device as in claim 19, wherein the ring is less doped than the sinker structure.

24. The device as in claim 18, wherein the ring is doped in the range of 10^{14}-10^{15}/cm^2.

25. The device as in claim 18, wherein the active area is created and enclosed by a LOCOS process.

26. The device as in claim 25, wherein the active area comprises a substrate and an epitaxial layer on top of said substrate.

27. The device as in claim 18, wherein the first conducting type is the p type.

28. The device as in claim 18, wherein the ring is created by masked ion implant.

29. The device as in claim 24, wherein boron is used as a dopant.

30. The device as in claim 18, wherein the ring has a rectangular, circular, oval, polygon, or partially open shape.

31. The device as in claim 18, wherein the ring comprises at least one gap that does not substantially influence an insulating function of the ring.

32. A method of manufacturing a semiconductor device comprising the steps of:
- forming an active region of a first conducting type within a semiconductor material;
- forming a transistor structure, and
- forming a ring shaped region of the first conducting type extending from a surface of the active region into the active region and surrounding the transistor structure.

33. The method as in claim 32, wherein the step of forming a transistor structure comprises the steps of forming a drain region of a second type, a source region of the second type arranged along one side of the drain region, and a sinker structure of said first conducting type arranged substantially along said source region reaching from the surface of the active area next to the source region to the bottom of the active area.

34. The method as in claim 33, further comprising the step of forming a second source region arranged on the respective opposite side of the drain region, and a first and second sinker structure of said first conducting type arranged substantially along said source regions reaching from the surface of the active area next to the respective source regions to the bottom of the active area.

35. The method as in claim 32, wherein the drain region is formed in such a way that it comprises a lightly doped drain region.

36. The method as in claim 33, further comprising the step of arranging a metal layer on the backside of the semiconductor device.

37. The device as in claim 32, wherein the step of forming the ring includes the step of doping the ring less than the sinker structure.

38. The method as in claim 32, wherein the ring is doped in the range of 10^{14}-$10^{15}/cm^2$.

39. The method as in claim 32, wherein the active area is created and enclosed by a LOCOS process.

40. The method as in claim 32, wherein the ring is created by masked ion implant.

41. The method as in claim 32, wherein boron is used as a dopant.

42. The method as in claim 32, wherein the ring has a rectangular, circular, oval, polygon, or partially open shape.